Transient Thermal Simulation of High Power LED and its Challenges

Sanchit *Tandon*[1,2*], E *Liu*[2], Thomas *Zahner*[1], Sebastian *Besold*[1], Wolfgang Kalb[1], Gordon *Elger*[2*]
[1]OSRAM Opto Semiconductors GmbH, Regensburg, Germany
[2] Technische Hochschule Ingolstadt, Germany
*Corresponding Authors: sat2559@thi.de, +4917667054570, gordon.elger@thi.de, +498419348284

Abstract

Transient thermal analysis (TTA) is widely used to measure the transient thermal impedance (Z_{th}) and the thermal resistance of LEDs because reliability and lifetime of LED depends critically on junction temperature. To predict up-front in the product development process the lifetime of LED modules, calibrated finite element (FE) models are used. In this paper a FE-model for a family of high power LED is developed, i.e. different number of LED dies on ceramic sub-mounts of different sizes and calibrated to the Z_{th} measurements. Based on the CAD data for the selected LED module (two LED dies on ceramic carrier), different modern FE tools (ANSYS, Comsol and Flo-EFD) are used for transient FE simulation and benchmarked. All tools deliver appropriate results when best practice FE modeling is applied i.e. mesh quality, correct boundary condition, material data and contact resistances. To model the Z_{th} (t) measurement correctly, the suited approach of thermal boundary condition is investigated and a temperature boundary condition is proven as correct, practical and numerical efficient approach. The specific effect of heat generated in the converter of white LEDs on the transient impedance curve is revealed and investigated. Afterwards one FE-tool is coupled with the commercial optimizer OptiSLang. Based on available material data the FE model of the 2-chip LED module is calibrated to the experimental measured transient impedance curve. The calibrated model parameters are used to simulate the Z_{th} (t) curves of another high power LED module of this family. It was found that the simulated curves matched the experimental Z_{th} (t) curves of the LED modules. This validates the calibrated material properties for this entire LED family.

1. Introduction

The degradation of light-output and thereby the lifetime of LED systems depends on the junction temperature [1, 2, 3]. Thermal resistance R_{th-JC} (JC: junction to case) measurements of LED's are of vital importance and irrespective of the application industry-wide accepted. Transient thermal testing is the dominating method for measuring the transient thermal impedance Z_{th} and the R_{th-JC}. The method is described in the JEDEC 51-x family, e.g. the dual interface measurement for determination of the R_{th-JC} of electronic devices in JEDEC 51-14 [4] and in JEDEC 51-51 the application on LEDs, i.e. the determination of the real R_{th-JC} of LEDs [5].
High power LED modules are mounted on a heat sink. In dependence of the application and the operation condition the temperature of the heat sink may vary. For testing a standardized temperature, i.e. 25°C, is chosen. Heat sink and ambient are set to 25°C. For an LED module, the so called case temperature T_C is defined as the temperature of the heat sink under the LED module. For real heat sinks the T_C is the maximum temperature of the heat sink because the maximum temperature will be reached in the center under the LED module. In a transient thermal measurement set-up T_C is measured, i.e. a thermocouple is placed in the center under the LED module. In a typical test set-up the heat is transferred by an active thermo-electric cooler followed by a finned heat sink and a fan for forced convection. The temperature is controlled that the thermocouple directly under the LED module is kept constant on 25°C. When modeling the scenario, the real experimental conditions have to be translated into thermal boundary conditions. The importance of boundary condition for measuring the thermal resistance of LED packages is discussed and investigated using steady state simulation by Schweitzer [6]. It is shown that the R_{th-JC} is not an intrinsic property of the device but rather dependent on the junction temperature which is indeed dependent on the boundary conditions although the relation of dependency between R_{th-JC} with boundary condition is small. This might be at first astonishing but is well understandable when considering that the heat distribution and heat flux in the package change with the boundary condition. With the change in heat flux the effective area for heat transfer gets changed and therefore also the thermal resistance of the LED module. Therefore a standardized measurement method is needed to measure worldwide the same R_{th}. This is actually realized by sufficient large heat transfer of the active cooling and good thermal conductivity of the active cooling plate.
The thermal modeling process in the paper is started by investigating the boundary conditions and the impact of the boundary conditions on the Z_{th} curve. The result of the investigation is actually the known strategy: Moving the boundary condition sufficient far away from the part of the model which is of interest and post-processed. However, in the end, it had to be proven that the active cooling system behaves like the boundary conditions. Afterwards, the mesh dependency of the post-processed results was investigated and it was shown that mesh dependency is converging for fine meshes and well below experimental errors.
Nowadays, many different FE-tools are applied for thermal analyzes using different solvers. Therefore it is shown that three commercial FE tools (ANSYS, COMSOL and FloEFD) deliver the same results when appropriate best practice modelling is done.
Every simulation model has to be calibrated to experimental data. In most cases solely steady state models are used. However for LED analysis the transient thermal impedance is measured. Therefore, in the paper the time dependent cooling curves are fitted to the measured data. In the paper a commercial optimizer, i.e. OptiSLang is coupled to the FE tool. Different optimizing strategies are discussed presently

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for LED analysis and are investigated. However, in the paper a straight forward linear regression to minimize the sum of squared errors over all time steps is already able to do the job. The simulation parameter, i.e. material data is optimized in their respective ranges. Parameters are optimized in the reasonable ranges. Material properties are considered to be temperature independent for the simulation.

The real benefit of the developed simulation model is the application on a full LED module family. The calibration is done for one LED package of the family. The obtained parameter is then used to predict the Z_{th} curve of other members of the family. Care need to be taken to keep the mesh quality and mesh independence for the changed geometry.

The investigated device family is a white LED-module for automotive headlamps consisting of 2-5 LED chips on a ceramic carrier. The carrier is attached directly to an insulated metal substrate (IMS).

After model calibration a LED specific effect related to the converter of white LEDs was found. It was simulated that the transient thermal impedance depends on the converter. This is evident, however usually ignored for interpretation of the transient thermal impedance curve. The effect of different converter layers was simulated and validated experimentally. The paper discusses also the impact and the importance of these results.

2. Transient Thermal Analysis and Transient Simulation

Today transient thermal measurement is a standard measurement method for the transient thermal impedance $Z_{th}(t)$ and the thermal resistance R_{th} [8]. The forward voltage of the junction is measured as function of time after switching off the electrical (and thermal) load. The temperature T_j of the junction is obtained because the V_f depends in a sufficient small temperature range ($\Delta T<30°C$) linearly on the temperature. The sensitivity *s*, i.e. the proportional factor between forward voltage and temperature (for LEDs *s* is roughly around -2mV/K), has to be measured in an independent measurement. Following the JEDEC51-14 and JEDEC51-51 standard, the transient thermal impedance $Z_{th}(t)$ is obtained by the difference of the temperature of the junction $\boldsymbol{T_j(0) - T_j(t)}$ after switching off the thermal load P_{th} divided through the thermal load P_{th}:

$$\boldsymbol{Z_{th}(t) = \frac{T_j(0)-T_j(t)}{P_{th}} = \frac{1}{s}\frac{V_j(0)-V_j(t)}{P_{th}}} \quad (1)$$

T_j (t=0) denotes the temperature which is reached when the thermal load is applied. The V_f(t=0) however denotes the forward voltage measured after a short experimental dead time due to parasitic electrical effects of the measurement equipment and the electrical response of the forward voltage when switching the drive current. For measurement a commercial T3Ster Equipment from MICRED is used. The total thermal resistance R_{th} of the LED module under test is obtained for $\boldsymbol{t \to \infty}$ i.e. for larger times

Within the transient thermal FE simulation the same approach is followed. For cooling down simulation, at first a steady state simulation is performed applying the thermal load P_{th}. The temperature distribution is taken as initial temperature distribution of the simulated device under test. The heating power is switched off and the cooling down of the LED is simulated.

For post processing the temperature of the nodes in the epitaxial layer is used to calculate the junction temperature. The boundary conditions of the FE-model are discussed in the next sections.

3. Numerical Model and Boundary Conditions

The numerical model of the LED module was built based on the material and geometrical data as given in the data sheet. The basic structure of the high power LED is shown in *Figure* 1. The LED chips with die area of 1mm² are soldered on to a ceramic carrier, which is mounted using adhesive material on to an insulated metal substrate printed circuit board (IMS). In the simulation the cold plate is simulated as thick copper plate. The copper plate is connected to the IMS with a thermal interface material (TIM: Thermal grease) as thin interface between them. The boundary condition, i.e. temperature boundary condition of 25°C or heat transfer boundary condition are attributed to locate on the bottom of the copper plate and by that far enough away from the LED module and T_{case}. All other surfaces were treated as adiabatic, i.e. no heat exchange. The bonding between the LED chip and converter layer was considered as a thin resistive layer in the CAD model. The model was simplified and also e.g. bond wires, side coating and frame were neglected. All the thermal conductivities were considered to be isotropic in nature and temperature independent for the simulation.

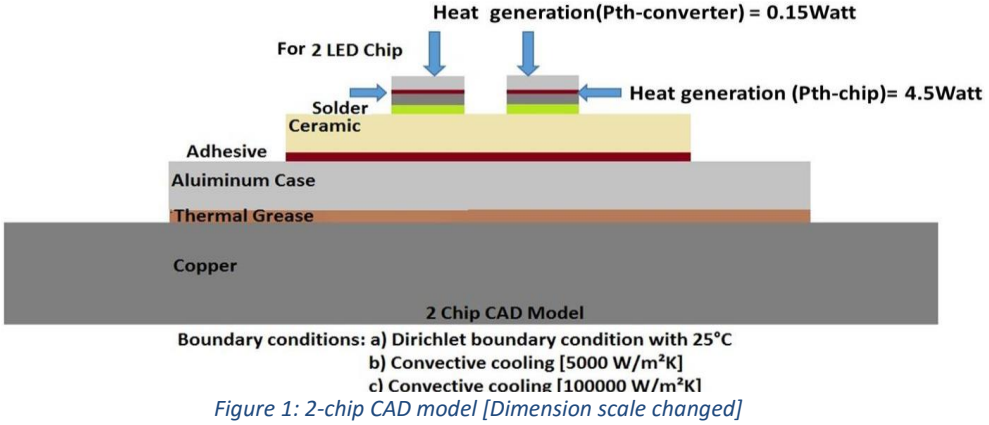


Figure 1: 2-chip CAD model [Dimension scale changed]

The electrical load (P_{el}) of 3 Watt for each chip was applied and a value of 25 % was assumed as optical efficiency. The $P_{th\text{-}chip}$ i.e. heat generated at the chip this is 75 % of P_{el} eg. 2.25 W. This thermal power is homogeneously applied on the cells representing the EPI. The phosphor converter is highly efficient. Quantum yield is close to 100%. However a thermal load is generated in the converter due to the transformation of blue light into light with longer wavelength. This heat load depends therefore on the color of the LED, i.e. the used converter. For the white LED under investigation 10% of the optical power emitted by the LED die is assumed to be lost as heat in the phosphor at the conversion process. The heat in the converter is modeled as homogeneously distributed in the cells representing the converter. The distribution of the thermal load is represented in *Figure* 2.

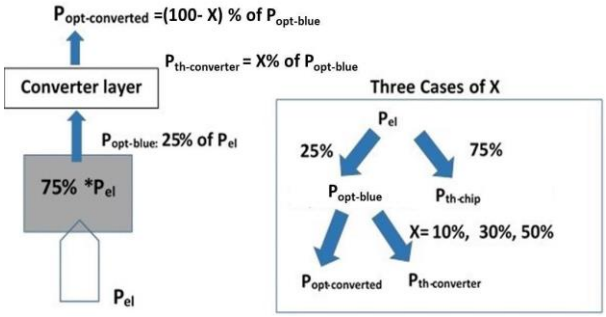


Figure 2: Thermal load distribution

Even when using powerful workstations, transient thermal simulations take a significant amount of time. Before starting with the transient thermal simulation , a suited level of mesh refinement needed to be established, i.e. fine enough that mesh dependency is below 1% but still usable in terms of computational time. The mesh dependency investigation was carried out for the steady state thermal simulation. The junction temperature was related to different meshing. The junction temperature referred is the maximum temperature which occurs in the epitaxial layer and the same is used for post processing for all the simulations. The case temperature T_{case} is the maximum temperature of the heat sink, i.e. of the temperature of the controlled cold plate in the measurement. In literature it is discussed about the dilemma of using average T_J or maximum T_J [6, 9]. Which is the better approach depends on the EPI design and the I-U characteristic curve.

The mesh size and the results of the mesh dependency are shown in *Figure* 3 and *Table* 1. Due to the small mesh dependency the transient simulation were performed using fine mesh type with a reasonable solution time and output result

Element Size [in meter]										
Mesh Type	Chip	Converter	Solder	Ceramic	Adhesive	Al-IMS	TIM	Heat Sink	T_j [°C]	Nodes
Very fine	3,00E-05	3,00E-05	3,00E-05	3,00E-05	3,00E-05	3,33E-04	3,33E-03	3,33E-03	39,202	3560409
Fine	3,00E-05	3,00E-05	3,00E-05	3,00E-04	3,00E-04	3,33E-03	3,33E-03	3,33E-03	39,167	135880
Coarse	1,66E-04	1,66E-04	1,66E-04	8,17E-04	8,17E-04	3,33E-03	3,33E-03	3,33E-03	39,121	5602
Change in T_j (Junction temperature) from finest to coarse mesh type is 0.2% which is very less										

Table 1: Mesh refinement study

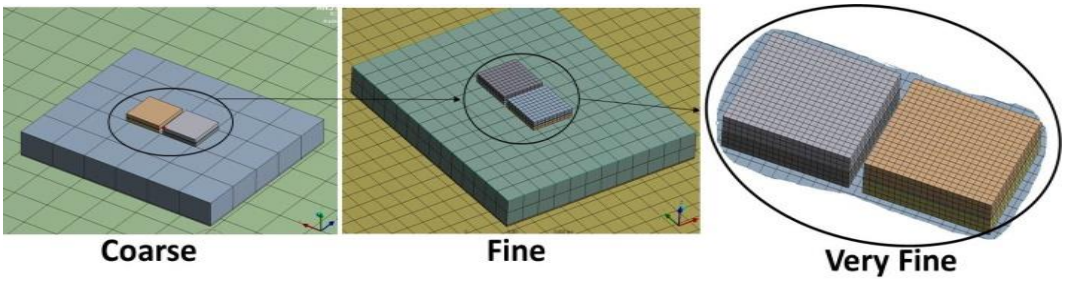


Figure 3: Mesh refinement at LED die level

3.1 Boundary Conditions

It's important to understand the experimentally cooling conditions for the transient temperature measurements. Temperature or heat transfer boundary conditions directly under the module are not adequate: Due to the temperature regulation, the heat transfer in the measurement from the LED module is changed that T_{case} remains constant 25°C. The boundary condition for simulation should provide sufficient cooling to make LED module properly heat sunk at the case as described in JEDEC standard.

One way of modelling would be a heat transfer condition under the module which is controlled by a subroutine to keep T_{case} constant. However, the same effect can be reached by modelling the temperature controlled table by a very good thermal conduction solid and a temperature boundary condition at the bottom of the solid. Different boundary cases were used. To investigate the impact of the boundary condition on the Z_{th} (t) different boundary conditions are chosen and tested.

Case 1: Constant temperature at lower surface of a copper heat sink. This fix boundary condition is the perfect realization of the case temperature to be perfectly heat sunk with no variation of temperature across the bottom surface. However this ideal condition is not realized by a real cooler which is better modelled by heat transfer conditions.

Case 2: Heat transfer conditions at lower surface of the heat sink with heat transfer coefficient of 5000W/m²K.

Case 3: Heat transfer conditions at lower surface of the heat sink with heat transfer coefficient of 100000W/m²K.

The thermal impedance curve shape is equal for all the boundary conditions (See *Figure* 4). For three boundary conditions, a small difference occurs at the later part of the curve which is approximately 0.0311K/W i.e. 1.02 %.

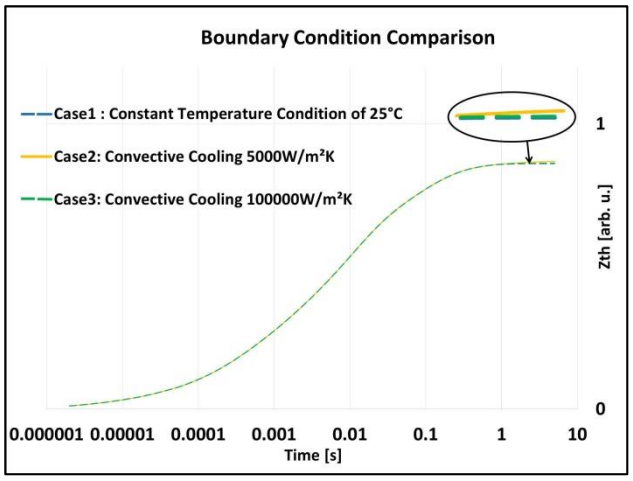
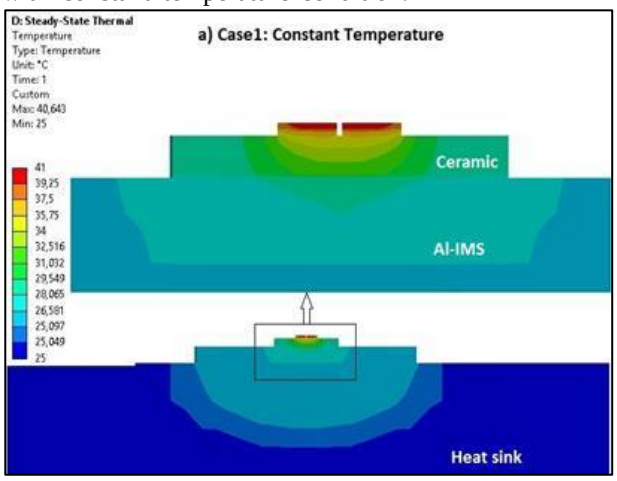
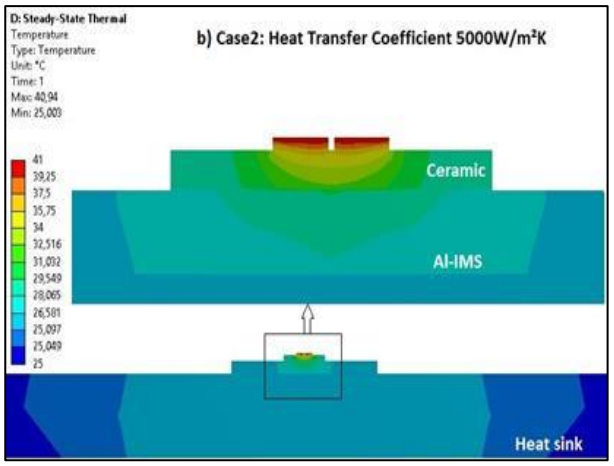


Figure 4: Boundary condition comparison (Note: All thermal impedance curves are normalized to measurement Rth value and arb.u. stands for arbitrary unit)

This difference in the thermal impedance curves can be easily explained as the boundary conditions effect the heat spreading into heat sink as can be seen in the *Figure* 5. Because the heat spreading and heat distribution in the LED module is the same until the heat sink the initial curve relates closely to one another for different boundary conditions. As there is no significant difference in the thermal impedance curve further simulations are done with constant temperature condition.





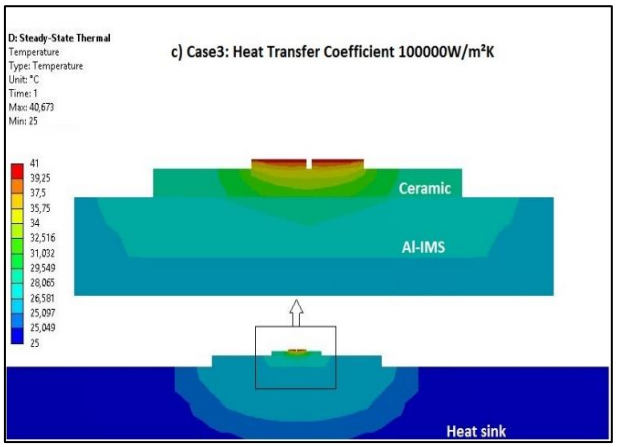


Figure 5: a) Case1: Temperature distribution of Heat sink; b) Case2: Temperature distribution of heat sink; c) Case3: Temperature distributions of heat sink. The difference in the temperature distribution can be seen at heat sink.

4. FE Tools Comparison

Different FE tools (Ansys Workbench, FloEFD and Comsol Multiphysics) were used to validate the model and the results were compared. Modelling options, i.e. modelling thin resistive layers and time steps are almost equal in the different FE-tools. The results obtained are quite similar. The slight differences can be the impact of different meshing method and mesh size in the different software's. The difference in modelling the thin resistive layer can also result in minor changes in the simulation results. In addition different solvers used by the FE Tools can result in a slight variance as shown in the Figure 6. This validation of the transient FE simulation in different FE tool proves that sufficiently comparable results are obtained when fine tuning the FE models and following the best practices of mesh refinement which in this case was done for Ansys workbench.

There was a difference of 1.2% in the final thermal impedance value of Comsol Multiphysics and Ansys workbench which can be due to meshing, thin restive layer and solver differences. Any FE tool can be used for the calibration process.

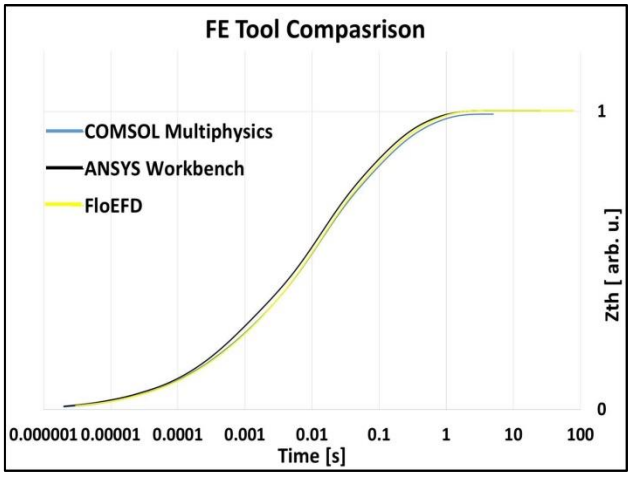


Figure 6: FE Tool Comparison (Note: All thermal impedance curves are normalized to measurement Rth value and arb.u. stands for arbitrary unit)

Ansys workbench was selected on the basis of the OptiSLang optimizer plug-in for Ansys workbench which is a much faster way to get the results for calibration.

5. Effect of Thermal Load Distribution at Converter layer

The distribution of the heat load on the EPI and the converter layer (see figure 2), i.e. different optical efficiency of the phosphor layer and light conversion at the converter, influences the simulated Z_{th} (t) curves significantly. Different converter types (warm or cold white light) change the Z_{th} (t) curve even if the thermal path from junction to case remains the same. However, for the overall thermal resistance $R_{th\ (j\text{-}case)}$ the distribution of the thermal load has no influence because all thermal flux is passing through the EPI layer and the steady state simulation will deliver the same result. For calibration the thermal model to the Z_{th} (t) curve the impact of the thermal load distribution is important and the effect is investigated and demonstrated in this section before discussing the numerical calibration approach.

The effect on the transient Z_{th} (t) curve based on various different converter layer efficiencies is simulated. Here converter efficiency refers to the amount of $P_{opt\text{-}blue}$ light converted to $P_{opt\text{-}white}$ converted. Three different converter efficiencies were considered (90%, 70% and 50%) as explained in *Figure* 2 and were then compared with the blue LED package, i.e. LED die with no phosphor conversion layer (*Figure* 7). The overall final thermal resistance of the device is same for all cases. However, the shape of the Z_{th} (t) curve is changed. The higher the converter efficiency the greater the slope of the impedance curve i.e. the rise of thermal impedance is faster.

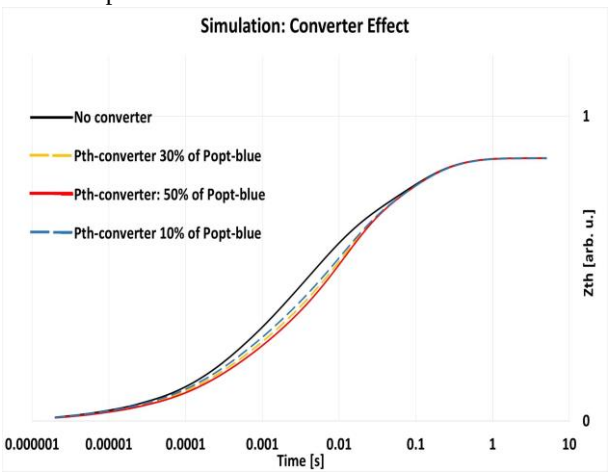


Figure 7: Comparison of different converter layer (Note: All thermal impedance curves are normalized to measurement Rth value and arb.u. stands for arbitrary unit)

The converter effect was found within the simulation and then reproduced by measurements. The converter layer was removed from one LED package and the Zth (t) curve was measured again. In figure 8 the measurement with and without converter is depicted revealing the same effect as visible in the simulation.

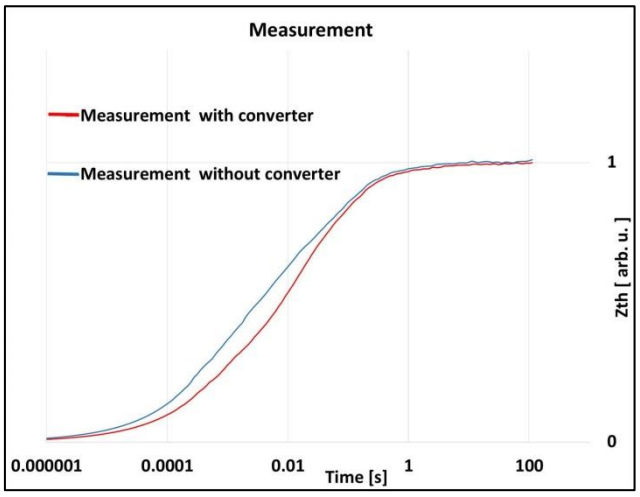


Figure 8: Measurement results shows similar effect for with and without converter (Note: All thermal impedance curves are normalized to measurement Rth value and arb.u. stands for arbitrary unit)

6. Calibration

The first comparison of results obtained from simulation using material properties from the data sheet gave a good agreement of the simulated curves with the measurement curve (see Figure 9) in the early time domain. Two thermal impedance curves are obtained after post processing average (Tj-avg) and maximum junction temperature (Tj-max) respectively. Tj-max for 2- chip module refers to the mean of maximum for both the LED dies on the ceramic substrate as they are symmetrical to each other. Tj-avg is the average temperature of the junction of the LED dies. The initial part of both simulated impedance curve fits well with measurement impedance curve. Whereas the impedance curve ($Z_{thTj\text{-}avg}$) for the Tj-avg deviates quiet early as compared to the impedance curve ($Z_{thTj\text{-}max}$) for Tj-max, approximately after 80 ms $Z_{thTj\text{-}max}$ also resulting in noticeable difference.

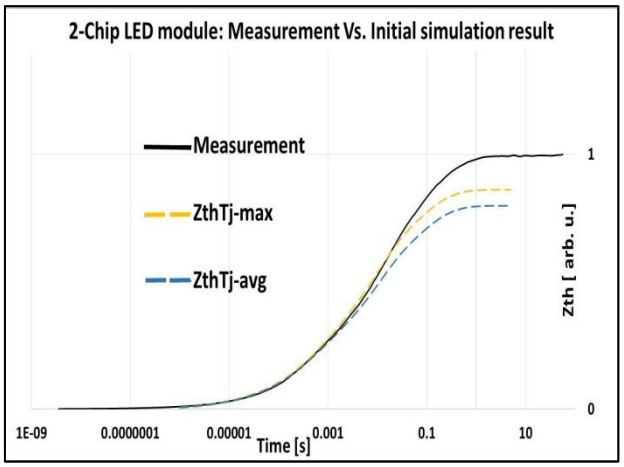


Figure 9: Measurement vs. Simulation for 2-chip LED module (Note: All thermal impedance curves are normalized to measurement Rth value and arb.u. stands for arbitrary unit)

Using the simulation thermal impedance curve for different component as shown in *Figure* 10. We can estimate which material property can help us to calibrate simulation to the measurement curve. The next step was to start with calibration process for the curve fitting based on the material properties as the parameters.

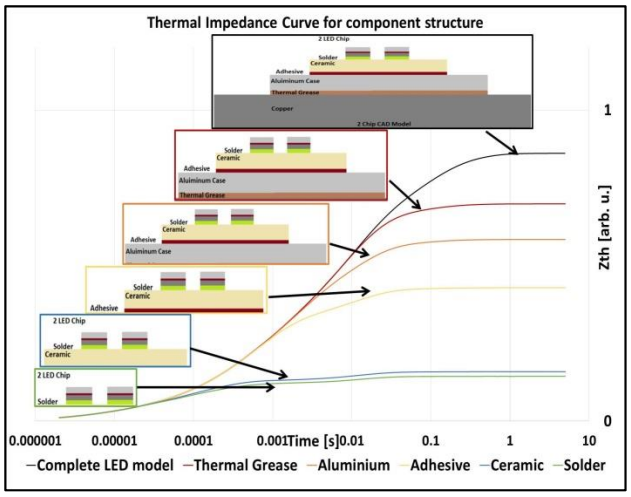


Figure 10: Structure wise thermal impedance curve (Note: All thermal impedance curves are normalized to measurement Rth value and arb.u. stands for arbitrary unit)

All the material properties of the LED package i.e. thermal conductivities and heat capacities of different components were chosen as parameters for the calibration so as to have a better agreement between measurement and simulation results. No geometric entities were changed. The geometry was validated by cross section of LED packages.

OptiSLang plugin in Ansys workbench was used to calibrate the simulated thermal impedance curve with the measurement thermal impedance curve. The sensitivity analysis was based on a design exploration. This was achieved using the design of experiments method (DOE) in which various design points are created using suitable sampling method which are available in the optimizer. The sampling method depends upon the number of parameters and decides the number of design points to explore the design space by varying the parameters within the range of parameters set by the user. The parameters value can be discrete values or set between a certain ranges. The list of parametrized inputs and the measurement results were fed into the optimizer using the extraction tool kit (ETK) which reads the data of all the nodes from the result file i.e. records the junction temperature within the Ansys workbench simulation.

Advanced Latin hypercube sampling technique was the base in our sensitivity analysis for selecting the design points within the pre-defined range of parameters for our calibration. The key behind this method as explained in [10] is stratification of input probability distribution. Stratification divides the cumulative curve into equal intervals and then a sample is randomly taken from each interval or stratification.

The schematic diagram in Figure 11 explains the flow for of the calibration process. The OptiSLang extraction tool read the result file from steady state and transient thermal simulation which are then used to evaluate the thermal impedance value i.e. Z_{th} (t). 30 design points (DP) were made using the Advanced Latin hypercube sampling method out of which the best design from the sensitivity analysis were selected for the impedance curves for Tj-max and Tj-avg. The Meta model of optimal prognosis (MOP) with Coefficient of Prognosis (CoP) automatically detects the most important parameters and provides the best possible meta-model.

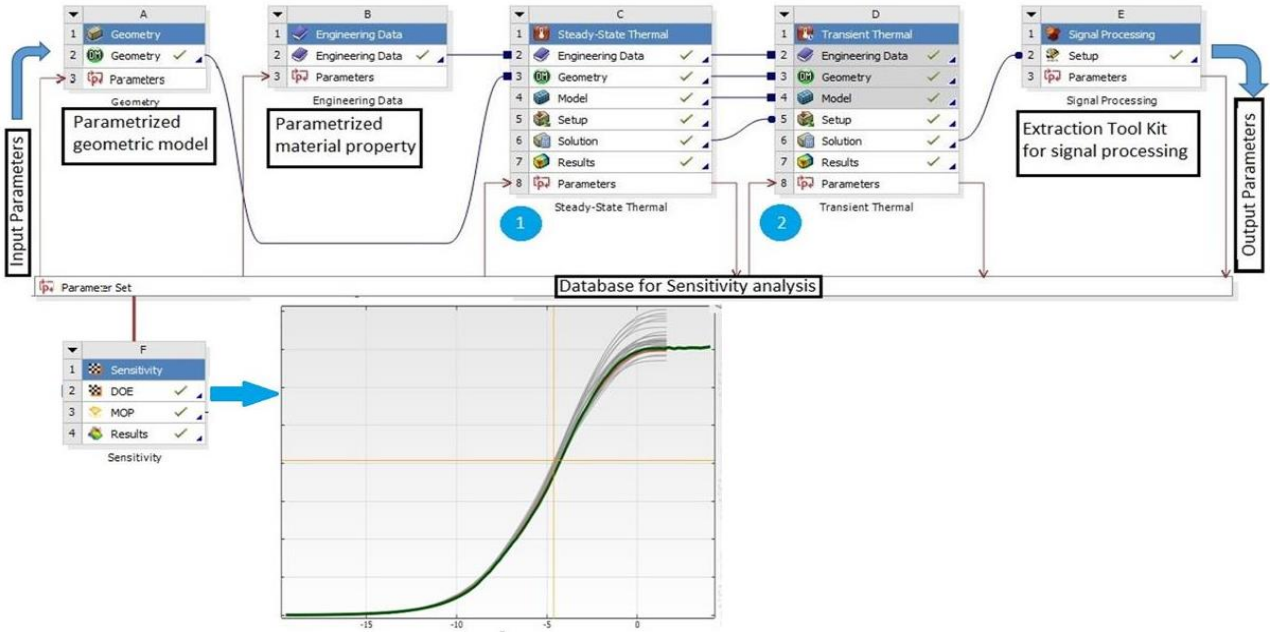


Figure 11: Schematic diagram for calibration process: The parametric material and geometric properties are given to step1 of simulation i.e. steady state thermal analysis to heat up the LED module till equilibrium is reached and then simulation step 2 i.e. transient thermal analysis where the cooling curve is measured after turning off the thermal load. These data are read by extraction tool kit (ETK) and result is stored for each design point in the database for sensitivity analysis. This is repeated for all the design points.

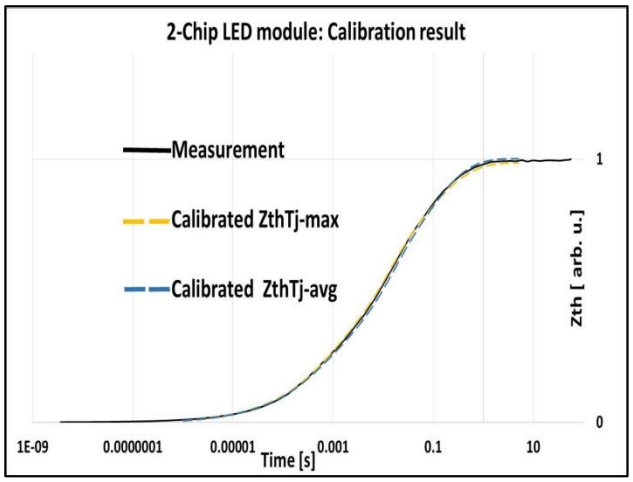


Figure 12: Calibration results for 2-chip LED module with Tj-max and Tj-avg (Note: All thermal impedance curves are normalized to measurement Rth value and arb.u. stands for arbitrary unit)

There are also different optimization techniques such as Downhill simplex, Evolutionary algorithm etc. which can be used to optimize the best design points from sensitivity results. Best design points (DP's) obtained from the sensitivity analysis is shown in *Figure 12*. Calibration results show good fitting for both ($Z_{thTj\text{-}max}$ and $Z_{thTj\text{-}avg}$) simulated impedance curves with the measurement impedance curve. The calibrated material properties for both the curves are different. Percentage changes in the thermal conductivities and heat capacities of the parameters from the initial material properties can be seen in *Figure* 13 and *Figure* 14 respectively.

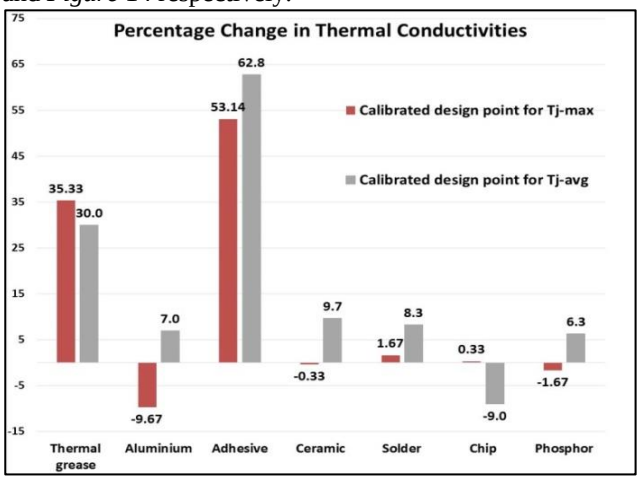


Figure 13: Percentage change in thermal conductivities for calibrated design points for $Z_{thTj\text{-}max}$ (t) and $Z_{thTj\text{-}avg}$ (t).

Note: negative changes mean increase in the value compared to initial material properties and positive changes mean decrease in the value.

The optimizer drastically changed the thermal conductivities of adhesive and thermal grease to get better fitting. There were changes in thermal conductivity of well-known components such as chip. These changes are most probably due to surface resistances which are not included in the model and lead to lower thermal conductivity when the bulk material is fitted. Also slight changes in the material properties of phosphor, aluminium and ceramic were observed. This can be because e.g. the thermal mass of the side coat was neglected in the model. So to overcome their effect the optimizer calibrated their effect on to existing materials and provided results of the impedance curve match very good with the initial part of measurement result.

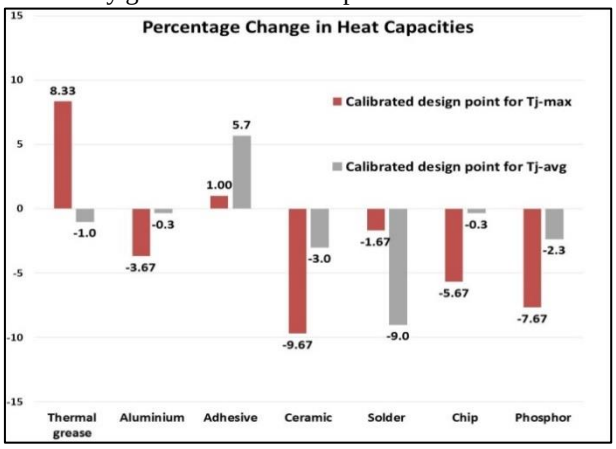


Figure 14: Percentage change in heat capacities for calibrated design points with for $Z_{thTj\text{-}max}$ and $Z_{thTj\text{-}avg}$.

These two parametric sets are now validated on another LED module belonging to same family but with different number of LED chips and different size of ceramic substrate.

7. Validation of the Calibration

5-chip LED module and 3-chip LED modules from the same family were then FE modelled based on dimensions in data sheet. Zth curves were also measured for 3-chip and 5-chip LED modules. The first simulation was carried out with the initial material properties and then with the calibrated sets of material property from the 2-chip calibrated module. The Z_{th} (t) curve of the 5-chip module was also measured and compared with the simulated results (see *Figure* 15 and 16). The $Z_{th\ Tj\text{-}max}$ (t), $Z_{thTj\text{-}mean\ of\ max}$ (t) and $Z_{thTj\text{-}avg}$ (t) for the 5 chip module were computed using the calibrated set of parameters from the 2-chip module. Here $Z_{thTj\text{-}max}$ (t) refers to the maximum temperature among the five chips i.e. the junction temperature of the third chip in the centre and $Z_{th}Tj\text{-}_{mean\ of\ max}$ (t) refers to mean value of the maximum junction temperature for all the 5 LED chips. Since in case of 2-chip LED module $Z_{thTj\text{-}max}$ (t) and $Z_{thTj\text{-}mean}$ of max (t) are same because of symmetry so they were not shown separately.

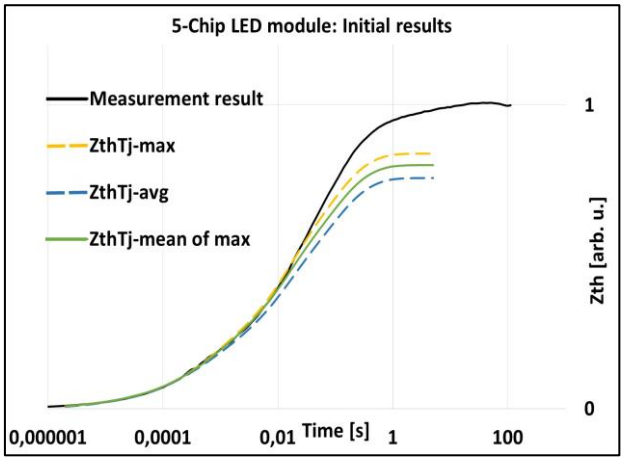


Figure 15: 5-Chip LED module initial simulation with initial material properties i.e. without the calibrated properties (Note: All thermal impedance curves are normalized to measurement Rth value and arb.u. stands for arbitrary unit)

As expected, the simulation with the initial parameter does not fit with the measurement result whereas the simulation

with the calibrated parameter from the 2-chip module shows very good fitting of the $Z_{thTj\text{-}avg}$ (t) curves for the 5-chip and 3-chip LED modules. Simulation and measurements of the 5-chip module are depicted in Fig. 16. For the 5-chip LED module the $Z_{th\ Tj\text{-}max}$(t) matches with the measurement result but the $Z_{th\ Tj\text{-}mean\ of\ max}$(t) fits until approximately 40 milliseconds. However, the LEDs are in series and the average of the maximum temperatures of the LED should represent the Z_{th} curve and not the overall maximum temperature. Therefore the maximum temperature post processing is under further evaluation. However, for the average temperature post processing approach (Tj-avg) the parameter calibration is valid also for the 5-chip module and the calibration is therefore validated for the overall family.

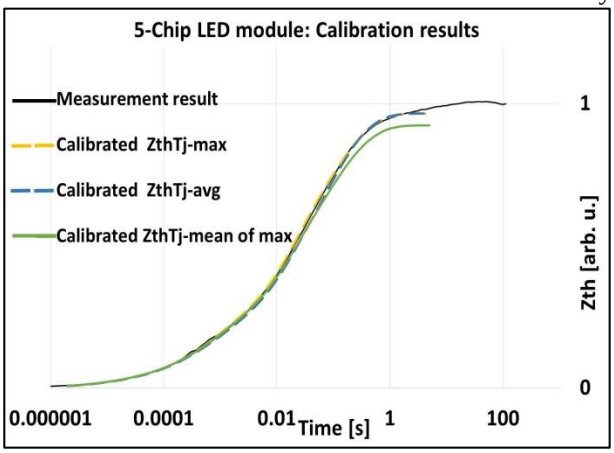


Figure 16: Validation of the calibrated material properties with 5-Chip LED module (Note: All thermal impedance curves are normalized to measurement Rth value and arb.u. stands for arbitrary unit)

8. Conclusion

This paper demonstrates calibration of thermal FE models to the transient thermal impedance curve for a LED family. Modern optimizers allow reducing the calibration work-load for the engineers by a factor of 10. As soon as the calibration work-flow is set-up the engineer hours needed for calibration are low and computational time of a standard workstation is solely in the range of several days. Any modern FE tool can be used as long as it allows coupling with optimizers which are able for CAD and thermal parameter access and simulation automation. Transient thermal FE model calibration should be seen as the new state of the art for thermal modelling of semiconductors.

The accuracy of calibration for LEDs can be improved by parameter separation, e.g. calibrating the blue LED package first followed by controlled modification (converter attachment, glob top). Further investigation for appropriate temperature data post processing will be performed. Taking the average temperature of the EPI layer gives appropriate results for LED packages under investigation. For thermal analysis of white LEDs the findings of the recent years, i.e. the impact of the converter on the Z_{th} (t) curve has to be implemented to avoid misinterpretation of the structure function and the thermal interfaces.

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